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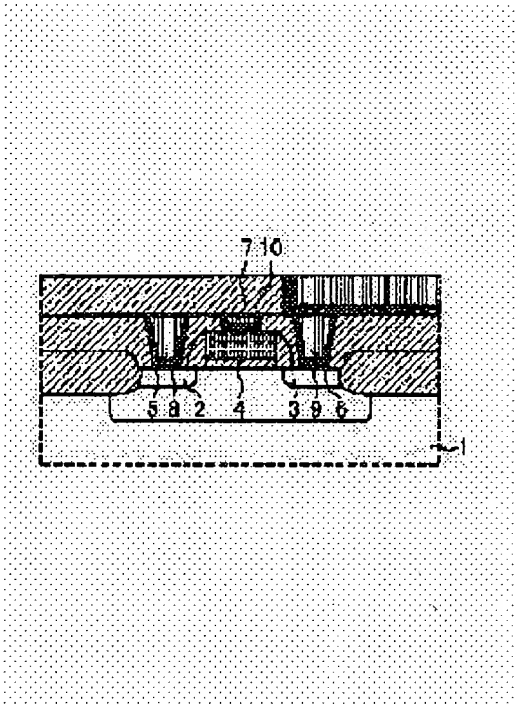
(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent Cu from diffusing from a Cu embedding wiring layer or a Cu plug by providing plural barrier layers between a first layer which is constituted of a first material and a second layer constituted of a second material and by making elements excepting the elements, which constitute the first and the second material, to mix with the barrier layers.

SOLUTION: One of first layers 2, 3 and 4 which are constituted of a first material or second layers 5, 6 and 7 constituted of a second material, is formed by Cu or metal including Cu and barrier layers 8, 9 and 10 are formed between the first layers 2, 3 and 4 and the second layers 5, 6 and 7 respectively. Elements excepting the elements which constitute the first and the second material are made to mix with these barrier layers 8, 9 and 10. That is, a compound is generated by reacting the elements, which constitute the first and the second material diffused into each barrier layer 8, 9 and 10 from a semiconductor active region and so on and the elements which are mixed with each of the barrier layers 8, 9 and 10.



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* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] the thing concerning [this invention] a semiconductor device and its manufacture approach -- it is -- especially -- Cu deposit -- CMP (Chemical Mechanical Polishing) -- it is related with the semiconductor device which has the description in the configuration of the barrier layer for raising the electromigration resistance of the plug embedded in the crevice by law, and an embedded wiring layer, and its manufacture approach.
[0002]
[Description of the Prior Art] Although the wiring layer by aluminum alloy is mainly conventionally used as a wiring layer of a semiconductor device, in order to solve the problem of the increment in the resistance accompanying detailed-izing of a wiring layer, and the life of a wiring layer, use of Cu which is low resistance and excelled aluminum in electromigration resistance is considered.
[0003] since the suitable gas which etches Cu by the high selection ratio to the insulator layer used as a substrate in the dry etching approach required for micro processing does not exist when forming the detailed wiring layer using such Cu -- DAMASHIN (Damascene) -- it is in use to form an embedded plug and embedded wiring layer structure by law.
[0004] this DAMASHIN -- law -- an insulator layer -- crevices, such as a wiring groove or a contact hole, i.e., a beer hall etc., -- preparing -- the whole surface -- electric-field plating -- or After making thick Cu layer deposit with the CVD method using Cu(hfac) TMVS etc., Cu layer deposited on fields other than a crevice using the CMP method is removed. It is observed as a technique which can form Cu embedded wiring layer or Cu plug embedded in the crevice, and can form uniform wiring in the size below submicron one.
[0005] Here, with reference to drawing 7 and drawing 8 , the production process of the semiconductor device using the conventional embedded wiring process is explained.
Drawing 7 (a) After forming the isolation oxide film 42 by giving selective oxidation to n mold silicon substrate 41 first 3 **, A field 43 is formed. some component formation fields surrounded by the isolation oxide film 42 -- p mold impurities, such as B, -- alternative -- introducing -- p mold -- a well -- subsequently It is SiO2 to the flank of the gate electrode 45 after forming the gate electrode 45 which consists of gate oxide 44 and polycrystal Si. The sidewall 46 which consists of film is formed. Subsequently After introducing n mold impurities, such as P (Lynn), alternatively by using the isolation oxide film 42 and the gate electrode 45 as a mask and forming n mold source field 47 and n mold drain field 48, Thick SiO2 which serves as an interlayer insulation film 49 by the PCVD method (plasma chemistry vapor growth) The film is made to deposit.
[0006] Drawing 7 (b) 3 **, subsequently, after carrying out flattening of the front face of an interlayer insulation film 49 by grinding using the CMP method, n mold source field 47, n mold drain field 48, and the beer halls 50, 51, and 52 to the gate electrode 45 are formed by giving reactive ion etching (RIE) by using a predetermined resist mask (not shown) as a mask. In addition, it is formed in a location which is mutually different in fact, although beer halls 50, 51, and 52 are shown so that it may stand in a line in

the shape of a straight line in order to simplify illustration.
[0007] Drawing 7 (c) Subsequently, after making the TiN film 53 which serves as barrier metal by the sputtering method deposit on the whole surface, the thick Cu deposit 54 is made to deposit using electrolysis plating 3 **.
[0008] Drawing 8 (d) 3 **, subsequently, by the CMP method, it grinds until the front face of an interlayer insulation film 49 is exposed, and the Cu deposit 54 and the TiN film 53 which were deposited on beer halls 50 and 51 and fields other than 52 are removed, and the Cu plugs 55, 56, and 57 are formed.
[0009] drawing 8 (e)3 ** -- subsequently -- again -- PCVD -- SiO2 which serves as an interlayer insulation film 58 using law After making the film deposit, the wiring groove 59 for forming the wiring layer which contacts the Cu plugs 55, 56, and 57 electrically is formed, and, subsequently the TiN film 60 which serves as barrier metal by the sputtering method is made to deposit on the whole surface by giving reactive ion etching by using a predetermined resist mask (not shown) as a mask. In addition, in fact, although beer halls 50, 51, and 52 show the wiring groove 59 for the wiring layer linked to the Cu plug 56 to n mold drain field 48 in drawing since they are formed in a mutually different location, they also form the wiring groove to the Cu plugs 55 and 57 in other locations at coincidence.
[0010] Drawing 8 (f) 3 **, subsequently, after making thick Cu deposit deposit using electrolysis plating, by the CMP method, it grinds until the front face of an interlayer insulation film 58 is exposed, and Cu deposit deposited on fields other than wiring groove 59 and the Cu embedded wiring layer 61 which removes TiN film 60 and connects with the Cu plug 56 are formed. In addition, although not illustrated, Cu embedded wiring layer to the Cu plugs 55 and 57 is also formed in coincidence.
[0011] The multilayer-interconnection structure by Cu embedded wiring layer is formed by performing such a process also to Cu plug for taking connection with the upper wiring layer and the upper wiring layer if needed.
[0012]
[Problem(s) to be Solved by the Invention] However, the history of such a Cu embedded wiring layer is short, and there are many problems which are not yet actualized, for example, Cu is Si and SiO2. With the TiN film used as a barrier metal to the conventional aluminum wiring layer since the diffusion coefficient in inside is large, they are Si or SiO2. There is a problem that diffusion of Cu to the inside of the film cannot be prevented.
[0013] for example, when Cu is spread from Cu plug to Si, i.e., a source field, or a drain field SiO2 in which degradation of the component property of leakage current increasing will be caused to, and Cu constitutes Si or an interlayer insulation film from a Cu plug or a Cu embedded wiring layer By being spread into the film A void is formed in Cu plug or Cu embedded wiring layer, Cu plug and Cu embedded wiring layer deteriorate, and there is a problem that the life of Cu plug or Cu embedded wiring layer becomes short.
[0014] Therefore, this invention aims at raising a component property and the dependability of wiring layer structure by preventing diffusion of Cu from Cu embedded wiring layer or Cu plug.
[0015]
[Means for Solving the Problem] Drawing 1 is the explanatory view of the theoretic configuration of this invention, and explains The means for solving a technical problem in this invention with reference to this drawing 1 .
Drawing 1 reference (1) this invention is characterized by making elements other than the element which constitutes the 1st ingredient and 2nd ingredient in the barrier layers 8, 9, and 10 mix in the semiconductor device which has the multilayer structure which formed the barrier layers 8, 9, and 10 between the 1st layer which consists of the 1st ingredient, and the 2nd layer 5, 6, and 7 which consists of the 2nd ingredient.
[0016] Thus, by making elements other than the element which constitutes the 1st ingredient and 2nd ingredient mix in the barrier layers 8, 9, and 10 The element which constitutes the 1st ingredient and 2nd ingredient which have been diffused in the barrier layers 8, 9, and 10 from the 1st layer 2, 3, and 4 or the 2nd layer 5, 6, and 7, i.e., a semi-conductor active region, a semi-conductor diffusion wiring layer, a

semi-conductor wiring layer, a metal wiring layer, a metal plug, etc., Since the element mixed in the barrier layers 8, 9, and 10 reacts and a compound is generated, the element which constitutes the 1st ingredient and 2nd ingredient can control being spread more than it, and can prevent degradation of a component property, or the fall of a wiring life.

[0017] (2) Moreover, this invention is standard generation energy deltaf Hdegree1 at the time of the element made to mix in the barrier layers 8, 9, and 10 forming the element and compound which constitute the environmental impurity, the 1st ingredient, and the 2nd ingredient in the barrier layers 8 and 9 and 10 in the above (1). In 298 degrees C, it is characterized by being the element of deltaf Hdegree1 <=-600 kJ/mol.

[0018] Thus, standard generation energy deltaf Hdegree1 at the time of forming the element and compound which constitute the barrier layers 8 and 9 and the environmental impurity in ten, for example, oxygen, nitrogen or carbon, the 1st ingredient, and the 2nd ingredient, in order to control diffusion by generation of a stable compound In 298 degrees C, it is desirable to use the element of deltaf Hdegree1 <=-600 kJ/mol.

[0019] (3) Moreover, this invention is standard generation energy deltaf Hdegree2 at the time of generating a compound in the above (2) in standard generation energy deltaf Hdegree1, and the barrier layers 8, 9, and 10, the 1st layer 2, 3, and 4 or the 2nd layer 5, 6, and 7. It is characterized by having the relation of deltaf Hdegree1 <<deltaf Hdegree2.

[0020] Thus, it is the standard generation energy at the time of generating a compound, since it is required to be more more stable than the compound generated in the barrier layers 8, 9, and 10, the 1st layer 2, 3, and 4, or the 2nd layer 5, 6, and 7 in order to control diffusion by generation of a compound deltaf Hdegree2 When it carries out, it is desirable to have the relation of deltaf Hdegree1 <<deltaf Hdegree2.

[0021] (4) Moreover, this invention is characterized by at least one side of the 2nd ingredient which constitutes the layers 5, 6, and 7 of 1st ingredient **** 2 which constitutes the 1st layer 2, 3, and 4 being a metal containing Cu or Cu in the above (1) thru/or either of (3).

[0022] The diffusion phenomenon of the element which constitutes such the 1st layers 2, 3, and 4 or 2nd layer 5, 6, and 7 is remarkable when the 1st layers 2, 3, and 4 or 2nd layer 5, 6, and 7 consists of metals containing Cu or Cu.

[0023] (5) Moreover, in the above (1) thru/or either of (4), this invention is characterized by being either, although at least one layer of the barrier layers 8, 9, and 10 added Si to the metal which consists of Ti, Ta, or W, the nitride of Ti, Ta, or W, or the nitride of Ti, Ta, or W.

[0024] As barrier layers 8, 9, and 10, thus, Ti, Ta, Or the metal which consists of W, Ti, Ta, Or the nitride of W, for example, TiN, Ti, Ta, Or what added Si to the nitride of W, for example, Si content TiN film, That is, the TiSiN film is suitable and the metal which consists of Ti, Ta, or W to the embedded wiring layer which the diameter of crystal grain of the TiN film becomes small in nano size, and barrier resistance improves, and is prepared on an interlayer insulation film may be used by making Si contain.

[0025] (6) Moreover, it is characterized by the element which makes this invention mix in the barrier layers 8, 9, and 10 in the above (1) thru/or either of (5) containing As, Mo, Fe, or at least one element in S.

[0026] Since diffusion of Cu is the barrier layers 8, 9, and 10, for example, the grain boundary diffusion along the grain boundary of the TiN film, (if required) L-C.Park and K-B.Kim, Journal of Electrochemical Society, vol.142, p.3109, 1995 reference, Since a stable compound is formed for the element which is easy to generate Cu and a compound the barrier layers 8 and 9 and by making a grain boundary contain especially 10 inside in a grain boundary and diffusion is controlled Diffusion of Cu can be controlled by making the element which is easy to generate Cu and a compound mix in the barrier layers 8, 9, and 10.

[0027] And standard generation energy deltaf Hdegree1 at the time of forming a compound with Cu Since a reaction tends to occur so that it is low (refer to the above-mentioned reference), as an element made to mix in the barrier layers 8, 9, and 10 Standard generation energy deltaf Hdegree1 at the time of

forming a compound with Cu by using either As, Mo, Fe or S In 298 degrees C, it can be made deltaf Hdegree1 <=-600 kJ/mol.
[0028] standard generation energy deltaf Hdegree1 in 298 degrees C at the time of generating the oxygen which is an environmental impurity, and Cu compound of each element of As, Mo, Fe, and S here If association, a compound phase, and standard generation energy deltaf Hdegree1 (kJ/mol) in 298 degrees C are shown in order Association A compound phase Standard generation energy deltaf Hdegree1 Cu-O Cu2 O - 168.6 CuO - 157.3 Cu-As Cu3 As - 11.715 Cu3 AsO4 - 624.041 Cu3 2 (AsO4) -1522.558 Cu-Mo CuMoO4 - 911.694 Cu-Fe CuFe 2O4 - 967.968 Cu-S Being set to Cu2 OSO 4 927.593 is known. - (if required) D. The volume on R.Lied grade, CRC Handbook of Chemistry and Physics, 74thed., Chap.5, and "Data of heat of formation for Cu compounds" and CRC the volume Press, BocaRaton, floor line, 1993, and on E.A.Brandes, and SmithellsMetals Reference Book and 6th ed., Chap.8, Butterworth, London, and 1983 -- and Ihsan The volume on Barin, Thermochemical Data of Pure Substances, VCH Publisher, New York, 1989 reference.
[0029] Only with therefore, the oxygen and copper which are an environmental impurity although a combination reaction seldom occurs since standard generation energy is high -- As, Mo, and Fe -- or Cu3 AsO4 with standard generation energy low when S is added, Cu3 2 (AsO4), CuMoO4, CuFe 2O4, and Cu2 OSO4 etc. -- since a compound is generated and a grain boundary is filled with this compound, diffusion of Cu is controlled.
[0030] (7) Moreover, this invention is characterized by making the element made to mix in the barrier layers 8, 9, and 10 mix with ion-implantation in the approach of manufacturing the semiconductor device of the above (1) thru/or either of (6).
[0031] Thus, it is standard generation energy deltaf Hdegree1 to the barrier layers 8, 9, and 10. In case the element which forms a low compound is made to mix, it is desirable to use ion-implantation.
[0032] (8) Moreover, this invention is characterized by making the element made to mix in the barrier layers 8, 9, and 10 mix in the target used as the source of a spatter, or the source of vacuum evaporationo beforehand in the approach of manufacturing the semiconductor device of the above (1) thru/or either of (6).
[0033] Thus, it is standard generation energy deltaf Hdegree1 to the barrier layers 8, 9, and 10. In case a low element is made to mix, in the process which forms the barrier layers 8, 9, and 10 with the sputtering method or vacuum deposition, it is desirable to make the element concerned mix in the target used as the source of a spatter or the source of vacuum evaporationo beforehand.
[0034] (9) Moreover, this invention is characterized by making the element made to mix in the barrier layers 8, 9, and 10 deposit with the sputtering method or vacuum deposition into the front face of the barrier layers 8, 9, and 10 or the barrier layers 8 and 9, and 10 in the process on which the barrier layers 8, 9, and 10 are made to deposit in the approach of manufacturing the semiconductor device of the above (1) thru/or either of (6).
[0035] Thus, it is standard generation energy deltaf Hdegree1 to the barrier layers 8, 9, and 10. In case a low element is made to mix, an element may be made to deposit on the front face of the barrier layers 8, 9, and 10 with the sputtering method or vacuum deposition, or you may make it deposit in sandwiches into the barrier layers 8 and 9 and 10 in the process which forms the barrier layers 8, 9, and 10 with the sputtering method or vacuum deposition.
[0036] (10) Moreover, this invention is characterized by making the element made to mix in the barrier layers 8, 9, and 10 mix in the process which forms the barrier layers 8, 9, and 10 by the chemical-vapor-deposition method in the approach of manufacturing the semiconductor device of the above (1) thru/or either of (6).
[0037] Thus, it is standard generation energy deltaf Hdegree1 to the barrier layers 8, 9, and 10. In case the element which forms a low compound is made to mix, you may make it mix in the barrier layers 8, 9, and 10 by making the element concerned mix into a deposition ambient atmosphere in the process which forms the barrier layers 8, 9, and 10 by the chemical-vapor-deposition method, i.e., a CVD method.
[0038]

[Embodiment of the Invention] Here, although the gestalt of operation of the 1st of this invention is explained with reference to drawing 2 thru/or drawing 4 , drawing 2 and drawing 3 are the explanatory views of the production process of the gestalt of operation of the 1st of this invention, and drawing 4 is the explanatory view of the effectiveness in the gestalt of operation of the 1st of this invention.
Drawing 2 (a) After forming the isolation oxide film 12 by giving selective oxidation to n mold silicon substrate 11 like the conventional production process first 3 **, A field 13 is formed. some component formation fields surrounded by the isolation oxide film 12 -- p mold impurities, such as B, -- alternative -- introducing -- p mold -- a well -- subsequently It is SiO2 to the flank of the gate electrode 15 after forming the gate electrode 15 which consists of gate oxide 14 and polycrystal Si. The sidewall 16 which consists of film is formed. Subsequently PCVD after introducing P alternatively by using the isolation oxide film 12 and the gate electrode 15 as a mask and forming n mold source field 17 and n mold drain field 18 -- the thickness it is thin to an interlayer insulation film 19 with law -- for example, 0.8-micrometer SiO2 The film is made to deposit.
[0039] Subsequently, after carrying out flattening of the front face of an interlayer insulation film 19 by grinding using the CMP method, n mold source field 17, n mold drain field 18, and the beer halls 20, 21, and 22 to the gate electrode 15 are formed by giving reactive ion etching using the mixed gas which consists of C4 F8+CO+Ar by using a predetermined resist mask (not shown) as a mask. In addition, it is formed in a location which is mutually different in fact, although beer halls 20, 21, and 22 are shown also in this case so that it may stand in a line in the shape of a straight line in order to simplify illustration.
[0040] Drawing 2 (b) After making the thickness of 50nm deposit on the whole surface, subsequently the As ion 24 for the TiN film 23 which serves as barrier metal by the sputtering method 3 ** with the acceleration energy of 30keV The As ion 24 is mixed in the TiN film 23 by carrying out an ion implantation on condition that 1.0x1013-1.0x1015cm-2, 3x1014cm-2 [for example,], for example, performing heat treatment for 30 minutes in 400 degrees C.
[0041] Drawing 2 (c) Subsequently the thickness on an interlayer insulation film 19 makes the 1.5-micrometer Cu layer 25 deposit using the sputtering method 3 **.
[0042] drawing 3 (d) -- the Cu layer 25 which ground until the front face of an interlayer insulation film 19 was exposed, and was subsequently deposited on beer halls 20 and 21 and fields other than 22 by the CMP method 3 ** -- and it removes TiN film 23 and the Cu plugs 26, 27, and 28 are formed.
[0043] drawing 3 (e)3 ** -- subsequently -- again -- PCVD -- the thickness it is thin to an interlayer insulation film 29 using law For example, 0.8-micrometer SiO2 By giving reactive ion etching by using a predetermined resist mask (not shown) as a mask, after making the film deposit The wiring groove 30 for forming the wiring layer which contacts the Cu plugs 26, 27, and 28 electrically is formed. Subsequently After making the TiN film 31 which serves as barrier metal by the sputtering method deposit on the whole surface, again the As ion 32 with the acceleration energy of 30keV The As ion 32 is mixed in the TiN film 31 by carrying out an ion implantation on condition that 1.0x1013-1.0x1015cm-2, 3x1014cm-2 [for example,], for example, performing heat treatment for 30 minutes in 400 degrees C. In addition, also in this case, although beer halls 20, 21, and 22 show the wiring groove 30 for the wiring layer linked to the Cu plug 27 to n mold drain field 18 in drawing since they are formed in a mutually different location, they also form the wiring groove to the Cu plugs 26 and 28 in other locations in fact at coincidence. Moreover, it is thick SiO2 used as an interlayer insulation film 28 in fact. The about 50nm SiN film is made to deposit on the bottom of the film as an etching stopper layer.
[0044] Drawing 3 (f) 3 **, subsequently, using the sputtering method, by the CMP method, it grinds until the front face of an interlayer insulation film 29 is exposed, and thickness forms Cu layer deposited on fields other than wiring groove 30, and the Cu embedded wiring layer 33 which removes TiN film 23 and connects with the Cu plug 27, after making 1.5-micrometer Cu layer deposit. In addition, although not illustrated, Cu embedded wiring layer to the Cu plugs 26 and 28 is also formed in coincidence.
[0045] The multilayer-interconnection structure by Cu embedded wiring layer is formed by performing such a process also to Cu plug for taking connection with the upper wiring layer and the upper wiring

layer if needed.
[0046] Drawing 4 reference drawing 4 is n+ to p mold field, in order to check the effectiveness of the gestalt of operation of this invention. On the n+/p diode in which the mold field was formed The 50nm TiN film is deposited. After As ion implantation 200nm Cu film, Carry out the sequential deposition of the 50nm TiN film, and the electrode of TiN/Cu/TiN structure is formed. After performing annealing treatment for 30 minutes at 700 degrees C, the leakage current at the time of impressing the reverse bias of 2.5V is measured to this diode, and leakage current is shown in it as cumulative frequency distribution. When As ion is poured in so that clearly from drawing, leakage current decreases compared with the case where it does not pour in, especially leakage current in case an injection rate is 1x1014cm-2 or 1x1015cm-2 is about 1x10-9A, and leakage current reduces it sharply compared with abbreviation 1x10-6A [in / in the accumulation probability when not carrying out an ion implantation / 99%].
[0047] Therefore, it sets in the gestalt of operation of the 1st of this invention. Even if Cu is spread from the Cu plugs 26 and 27 during component actuation by having mixed As in the TiN film 23 the TiN film 23 -- setting -- Cu3 AsO4 and Cu3 2 (AsO4) etc. -- a compound is generated, and diffusion of Cu can be controlled when this compound fills the grain boundary of the TiN film 23.
[0048] Moreover, SiO2 of the Cu embedded wiring layer 33 For the perimeter which touches the film, since it is covered by the TiN film 31 by which As was mixed, Cu of the Cu embedded wiring layer 33 is SiO2. Since it is not spread in the film, therefore a void does not occur in the Cu embedded wiring layer 33, a wiring layer life does not fall.
[0049] Next, with reference to drawing 5 and drawing 6 , the production process of the gestalt of operation of the 2nd of this invention is explained.
Drawing 5 (a) After forming the isolation oxide film 12 by giving selective oxidation to n mold silicon substrate 11 like the gestalt of the 1st operation of the above first 3 **, A field 13 is formed. some component formation fields surrounded by the isolation oxide film 12 -- p mold impurities, such as B, -- alternative -- introducing -- p mold -- a well -- subsequently. It is SiO2 to the flank of the gate electrode 15 after forming the gate electrode 15 which consists of gate oxide 14 and polycrystal Si. The sidewall 16 which consists of film is formed. Subsequently PCVD after introducing P alternatively by using the isolation oxide film 12 and the gate electrode 15 as a mask and forming n mold source field 17 and n mold drain field 18 -- the thickness it is thin to an interlayer insulation film 19 with law -- for example, 0.8-micrometer SiO2 The film is made to deposit.
[0050] Subsequently, after carrying out flattening of the front face of an interlayer insulation film 19 by grinding using the CMP method, n mold source field 17, n mold drain field 18, and the beer halls 20, 21, and 22 to the gate electrode 15 are formed by giving reactive ion etching using the mixed gas which consists of C4 F8+CO+Ar by using a predetermined resist mask (not shown) as a mask. In addition, it is formed in a location which is mutually different in fact, although beer halls 20, 21, and 22 are shown also in this case so that it may stand in a line in the shape of a straight line in order to simplify illustration.
[0051] Drawing 5 (b) Subsequently the thickness of 50nm is made to deposit the Mo content TiN film 34 used as barrier metal on the whole surface 3 ** by carrying out sputtering of the Mo using 0.05 - 2.0%, for example, Ti target included 1.0%.
[0052] Drawing 5 (c) Subsequently the thickness on an interlayer insulation film 19 makes the 1.5-micrometer Cu layer 25 deposit using the sputtering method similarly 3 **.
[0053] drawing 6 (d) -- the Cu layer 25 which ground until the front face of an interlayer insulation film 19 was exposed, and was subsequently deposited on beer halls 20 and 21 and fields other than 22 by the CMP method 3 ** -- and it removes Mo content TiN film 34, and the Cu plugs 26, 27, and 28 are formed.
[0054] drawing 6 (e)3 ** -- subsequently -- again -- PCVD -- the thickness it is thin to an interlayer insulation film 29 using law For example, 0.8-micrometer SiO2 By giving reactive ion etching by using a predetermined resist mask (not shown) as a mask, after making the film deposit The wiring groove 30 for forming the wiring layer which contacts the Cu plugs 26, 27, and 28 electrically is formed. Subsequently The Mo content TiN film 35 used as barrier metal is made to deposit on the whole surface

again by carrying out sputtering of the Mo using 0.05 - 2.0%, for example, Ti target included 1.0%. In addition, also in this case, although beer halls 20, 21, and 22 show the wiring groove 30 for the wiring layer linked to the Cu plug 27 to n mold drain field 18 in drawing since they are formed in a mutually different location, they also form the wiring groove to the Cu plugs 26 and 28 in other locations in fact at coincidence. Moreover, it is thick SiO2 used as an interlayer insulation film 28 in fact. The about 50nm SiN film is made to deposit on the bottom of the film as an etching stopper layer.

[0055] Drawing 6 (f) 3 **, subsequently, again, by the CMP method, it grinds until the front face of an interlayer insulation film 29 is exposed, and thickness forms Cu layer deposited on fields other than wiring groove 30, and the Cu embedded wiring layer 33 which removes Mo content TiN film 35 and connects with the Cu plug 27 using the sputtering method, after making 1.5-micrometer Cu layer deposit. In addition, although not illustrated in this case, either, Cu embedded wiring layer to the Cu plugs 26 and 28 is also formed in coincidence.

[0056] The multilayer-interconnection structure by Cu embedded wiring layer is formed by performing such a process also to Cu plug for taking connection with the upper wiring layer and the upper wiring layer if needed.

[0057] Thus, since the Mo content TiN film 33 is used as barrier film, even if Cu is spread from the Cu plugs 26 and 27 during component actuation in the gestalt of operation of the 2nd of this invention, it sets on the Mo content TiN film 34, and it is CuMoO4. It is generated, and diffusion of Cu can be controlled when this compound fills the grain boundary of the Mo content TiN film 34.

[0058] Moreover, SiO2 of the Cu embedded wiring layer 33 For the perimeter which touches the film, since it is covered by the Mo content TiN film 35, Cu of the Cu embedded wiring layer 33 is SiO2. Since it is not spread in the film, therefore a void does not occur in the Cu embedded wiring layer 33, a wiring layer life does not fall.

[0059] As mentioned above, although the gestalt of each operation of this invention has been explained, this invention is not restricted to the configuration indicated in the gestalt of operation, and various kinds of modification is possible for it. For example, by using the TaN film or WN film instead of the TiN film, and making the TiN film, the TaN film, or WN film contain Si, or making Si contain, the diameter of crystal grain of the barrier film becomes small in nano size, and barrier metal can control diffusion of Cu along a grain boundary effectively.

[0060] Moreover, the barrier film is SiO2, although Ti film, Ta film, or W film is sufficient, and formation of silicide with Ti, Ta, and W becomes a problem when it prepares on Si. In the part which touches the film, since it is satisfactory, it can use as barrier film to the upper wiring layer.

[0061] Moreover, in explanation of the gestalt of each above-mentioned operation, as an element which the TiN film is made to contain, although As or Mo is used, Fe or S which forms the small compound of standard generation energy like As or Mo may be used.

[0062] Moreover, although ion-implantation or the sputtering method is used in explanation of the gestalt of each above-mentioned operation in case As or Mo is made to contain In using vacuum deposition or the MOCVD method (metal-organic chemical vapor deposition) and using vacuum deposition the element which forms the small compound of standard generation energy in the source of vacuum evaporationo is contained -- it makes -- ****ing -- moreover, MOVPE -- what is necessary is just to make the element which forms the small compound of standard generation energy into a growth ambient atmosphere contain, when using law

[0063] Moreover, although the element which forms the small compound of standard generation energy in the source of sputtering is made to contain in explanation of the gestalt of each above-mentioned operation and it is made to mix into [whole] the TiN film the element which forms the small compound of standard generation energy in case you may make it mix in sandwiches into the front face of the TiN film, or the TiN film and the TiN film is formed with the sputtering method or vacuum deposition -- independent -- sputtering -- or what is necessary is just to vapor-deposit

[0064] moreover, MOCVD using [in explanation of the gestalt of each above-mentioned operation, although Cu layer is made to deposit by the sputtering method, are not restricted to the sputtering method, and] electrolysis plating, an electroless deposition method, or Cu(hfac) TMVS -- you may

make it deposit by law In addition, when making Cu layer deposit with electrolysis plating, before making Cu layer deposit, it is desirable to make the thickness of 200nm deposit Cu seed film which serves as seed who can set like electrolysis galvanizer, and to use it as the substrate electric conduction film by the sputtering method.

[0065] moreover, PCVD which forms membranes at low temperature as an interlayer insulation film in explanation of the gestalt of each above-mentioned operation in consideration of the effect which it has on Cu plug and Cu embedded wiring layer -- SiO2 using law Although the film, i.e., the LTO film, is used not the thing restricted to the LTO film but FSG (fluorine content SiO2 film), and HSQ which is SOG of the inorganic system containing hydrogen -- or By using low dielectric constant film, such as an organic system insulator layer, and using such low dielectric constant film, the parasitic capacitance between wiring layers can be reduced and delay of a working speed can be prevented by it.

[0066] Moreover, in explanation of the gestalt of each above-mentioned operation, although pure Cu is used as Cu plug and a Cu embedded wiring layer as an interlayer insulation film, it is not restricted to pure Cu and the metal which uses as a principal component Cu(s), such as Cu alloy which doped other elements of Cu, may be used.

[0067] Moreover, in explanation of the gestalt of each above-mentioned operation, although Cu embedded wiring layer of the 1st layer linked to Cu plug and Cu plug is formed at another process, in the formation process of a beer hall, a wiring groove may also be formed in coincidence and Cu embedded wiring layer of the 1st layer linked to Cu plug and Cu plug may be formed in coincidence.

[0068] Moreover, in explanation of the gestalt of each above-mentioned operation, although IGFET (insulated-gate mold FET) is explained to an example as a semiconductor device, it is applied to other semiconductor devices including a bipolar transistor so that clearly also from the example of the diode of drawing 4 .

[0069]

[Effect of the Invention] Since the barrier film is made to contain the element which forms the small compound of standard generation energy, such as As, according to this invention in case Cu embedded wiring layer and Cu plug are formed Diffusion of Cu can be controlled by generating a compound with Cu. By it degradation of the operating characteristic of a component, or the fall of the life of a wiring layer -- it can decrease -- low -- the dependability of the semiconductor integrated circuit equipment of a high speed and a quantity degree of integration using Cu [****] as a wiring layer can be improved.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the explanatory view of the theoretic configuration of this invention.
[Drawing 2] It is the explanatory view of the production process to the middle of the gestalt of operation of the 1st of this invention.
[Drawing 3] It is the explanatory view of the production process after drawing 2 of the gestalt of operation of the 1st of this invention.
[Drawing 4] It is the explanatory view of the effectiveness in the gestalt of operation of the 1st of this invention.
[Drawing 5] It is the explanatory view of the production process to the middle of the gestalt of operation of the 2nd of this invention.
[Drawing 6] It is the explanatory view of the production process after drawing 5 of the gestalt of operation of the 2nd of this invention.
[Drawing 7] It is the explanatory view of the production process to the middle of the conventional semiconductor device.
[Drawing 8] It is the explanatory view of the production process after drawing 7 of the conventional semiconductor device.
[Description of Notations]
1 Semi-conductor Substrate
2 1st Layer
3 1st Layer
4 1st Layer
5 2nd Layer
6 2nd Layer
7 2nd Layer
8 Barrier Layer
9 Barrier Layer
10 Barrier Layer
11 N Mold Silicon Substrate
12 Isolation Oxide Film
13 P Mold -- Well -- Field
14 Gate Oxide
15 Gate Electrode
16 Sidewall
17 N Mold Source Field
18 N Mold Drain Field
19 Interlayer Insulation Film
20 Beer Hall
21 Beer Hall

22 Beer Hall
23 TiN Film
24 As Ion
25 Cu Layer
26 Cu Plug
27 Cu Plug
28 Cu Plug
29 2nd Interlayer Insulation Film
30 Wiring Groove
31 TiN Film
32 As Ion
33 Cu Embedded Wiring Layer
34 Mo Content TiN Film
35 Mo Content TiN Film
41 N Mold Silicon Substrate
42 Isolation Oxide Film
43 P Mold -- Well -- Field
44 Gate Oxide
45 Gate Electrode
46 Sidewall
47 N Mold Source Field
48 N Mold Drain Field
49 Interlayer Insulation Film
50 Beer Hall
51 Beer Hall
52 Beer Hall
53 TiN Film
54 Cu Deposit
55 Cu Plug
56 Cu Plug
57 Cu Plug
58 2nd Interlayer Insulation Film
59 Wiring Groove
60 TiN Film
61 Cu Embedded Wiring Layer

[Translation done.]

JAPANESE [JP,11-330001,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by making elements other than the element which constitutes said the 1st ingredient and 2nd ingredient in said barrier layer mix in the semiconductor device which has the multilayer structure which prepared the barrier layer between the 1st layer which consists of the 1st ingredient, and the 2nd layer which consists of the 2nd ingredient.
[Claim 2] Standard generation energy deltaf Hdegree1 at the time of the element made to mix in the above-mentioned barrier layer forming the element and compound which constitute the environmental impurity, the 1st ingredient of the above, and the 2nd ingredient in said barrier layer Semiconductor device according to claim 1 characterized by being the element of deltaf Hdegree1 <=-600 kJ/mol in 298 degrees C.
[Claim 3] The above-mentioned standard generation energy deltaf Hdegree1 Standard generation energy deltaf Hdegree2 at the time of generating a compound in the above-mentioned barrier layer, the 1st layer of the above, or the 2nd layer Semiconductor device according to claim 2 characterized by having the relation of deltaf Hdegree1 <<deltaf Hdegree2.
[Claim 4] A semiconductor device given in claim 1 characterized by at least one side of the 2nd ingredient which constitutes the layer of 1st ingredient **** 2 which constitutes the 1st layer of the above being a metal containing Cu or Cu thru/or any 1 term of 3.
[Claim 5] A semiconductor device given in claim 1 characterized by being either although at least one layer of the above-mentioned barrier layer added Si to the metal which consists of Ti, Ta, or W, the nitride of Ti, Ta, or W, or the nitride of Ti, Ta, or W thru/or any 1 term of 4.
[Claim 6] A semiconductor device given in claim 1 to which the element made to mix in the above-mentioned barrier layer is characterized by including As, Mo, Fe, or at least one element in S thru/or any 1 term of 5.
[Claim 7] The manufacture approach of the semiconductor device characterized by making the element which the above-mentioned barrier layer is made to mix in claim 1 thru/or any 1 term of 6 in the manufacture approach of the semiconductor device a publication mix with ion-implantation.
[Claim 8] The manufacture approach of the semiconductor device characterized by making the element which the above-mentioned barrier layer is made to mix in claim 1 thru/or any 1 term of 6 in the manufacture approach of the semiconductor device a publication mix in the target used as the source of a spatter, or the source of vacuum evaporationo beforehand.
[Claim 9] The manufacture approach of the semiconductor device characterized by making the element which said barrier layer is made to mix deposit into the front face of said barrier layer, or a barrier layer with the sputtering method or vacuum deposition in the process on which the above-mentioned barrier layer is made to deposit in the manufacture approach of a semiconductor device given in claim 1 thru/or any 1 term of 6.
[Claim 10] The manufacture approach of the semiconductor device characterized by making claim 1 thru/or any 1 term of 6 mix the element which the above-mentioned barrier layer is made to mix in the manufacture approach of the semiconductor device a publication in the process which forms said barrier

layer by the chemical-vapor-deposition method.

[Translation done.]